Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 74, 127 and 129 as follows:

Listing of Claims:

Claims 1-47. (Canceled)

48. (Previously Presented) A memory system, comprising:

a memory controller;

a memory bus operably coupled with the memory controller to communicate memory commands from the memory controller and communicate memory output signals to the memory controller; and

a plurality of memory modules operably coupled with the memory bus, the memory modules generating the memory output signals and responsive to the memory commands, at least some of the memory modules comprising:

an insulative substrate supporting a system interface;

a plurality of memory devices disposed on the insulative substrate;

a memory hub disposed on the insulative substrate and operably coupled with the memory devices and the system interface, the memory hub managing communications between the memory devices and the system interface in response to memory commands received via the system interface;

an activity sensing device monitoring activity of the memory module containing the activity sensing device in processing memory commands, the activity sensing device being operable to generate an output corresponding thereto; and

a module power controller coupled to the activity sensing device of the memory module containing the module power controller, the module power controller being operable to direct the memory devices in the memory module containing the module power controller to a reduced power state responsive to the output of the activity

sensing device indicating activity of the memory module containing the module power controller is not of a desired level.

49. (Original) The memory system of claim 48 wherein the module power controller directs the memory module to the reduced power state when the activity sensing device indicates memory module activity has fallen below the desired level.

50. (Original) The memory system of claim 48 wherein the module power controller directs the memory module to the reduced power state when the activity sensing device indicates memory module activity has exceeded the desired level.

51. (Original) The memory system of claim 48 wherein the module power controller is operable to determine when the memory module should be directed to the reduced power state responsive to the output of the activity sensing device.

52. (Original) The memory system of claim 48 wherein the module power controller is operable to direct the memory module to the reduced power state upon receiving an external reduced power signal.

53. (Original) The memory system of claim 48 wherein the module power controller of one of the memory modules comprises a master power controller, the master power controller receiving the output of the activity sensing device from at least one other memory module and, responsive to the output of the activity sensing device indicating activity of the memory module is not of the desired level, generates an external reduced power signal to direct the at least one other memory module to the reduced power state.

54. (Original) The memory system of claim 48 wherein the memory controller comprises a master power controller, the master power controller receiving the output of the activity sensing device from at least one other memory module and, responsive to the output of the activity sensing device indicating indicating activity of the memory module is not

of the desired level, generates an external reduced power signal to direct the at least one other memory module to the reduced power state.

55. (Original) The memory system of claim 48 wherein the memory module is directed to the reduced power state by the module power controller responsive to a single indication the activity of the memory module is not of the desired level reflected in the output of the activity sensing device.

56. (Original) The memory system of claim 48 wherein the memory module is directed to the reduced power state by the module power controller responsive to a plurality of indications the activity of the memory module is not of the desired level reflected in the output of the activity sensing device.

57. (Original) The memory system of claim 48 wherein the memory module is directed to the reduced power state by the module power controller when the output of the activity sensing device indicates the memory module has not received a desired number of memory commands for a predetermined time period.

58. (Original) The memory system of claim 48 wherein the activity sensing device comprises an activity monitor that monitors memory commands directed to the memory module.

59. (Original) The memory system of claim 58 wherein the activity monitor monitors the memory commands received via the system interface.

60. (Original) The memory system of claim 58 wherein the activity monitor comprises part of the memory hub.

61. (Original) The memory system of claim 48 wherein the activity sensing device comprises a temperature sensor wherein the temperature sensor is operable to

measure when the activity of the memory module is not of the desired level by monitoring temperature.

62. (Original) The memory system of claim 61 wherein the temperature sensor is operably coupled with at least one memory device to measure a memory device operating temperature.

63. (Original) The memory system of claim 61 wherein the temperature sensor is operably coupled with each of the memory devices to measure an aggregate memory device temperature.

64. (Original) The memory system of claim 61 wherein the temperature sensor is operably coupled with the insulative substrate to measure a memory module operating temperature.

65. (Original) The memory system of claim 61 wherein the temperature sensor is operably coupled with the memory hub to measure a memory hub operating temperature.

66. (Original) The memory system of claim 61 wherein the temperature sensor further comprises an ambient temperature sensor so that a measured temperature of the memory module can be compared to an ambient temperature.

67. (Original) The memory system of claim 48 wherein the plurality of memory devices comprise a plurality of DRAM devices.

68. (Original) The memory system of claim 67 wherein the reduced power state comprises a reduced refresh state in which memory cells of the DRAM devices are refreshed less frequently.

69. (Original) The memory system of claim 68 wherein the reduced refresh state comprises a self-refresh state.

70. (Original) The memory system of claim 48 wherein the reduced power state is a reduced response mode in which the module power controller limits response of the memory module to memory commands to control power consumption by the memory module.

71. (Previously Presented) The memory system of claim 70 wherein the module power controller limits the response of the memory module to memory commands by mandating idle intervals between responses to memory commands by the memory module.

72. (Original) The memory system of claim 48 wherein the output of the activity sensing device communicates that the memory devices of the memory module currently store no programming instructions and data, and the power management controller causes a plurality of devices of the memory module to be powered off.

73. (Original) The memory system of claim 48 wherein the output of the activity sensing device communicates that the memory devices of the memory module currently store programming information that has not been accessed by the system for an extended period, and the power management controller causes the contents of the memory devices to be saved to a storage device and a plurality of devices of the memory module to be powered off.

74. (Currently Amended) A computer system, comprising:

a processor;

an input device, operably connected to the processor, allowing data to be entered into the computer system;

an output device, operably connected to the processor, allowing data to be output from the computer system; and

a memory system, operably coupled with the processor, the memory system comprising:

a memory controller;

a memory bus operably coupled with the memory controller to communicate memory commands from the memory controller and communicate memory output signals to the memory controller; and

a plurality of memory modules operably coupled with the memory bus, the memory modules generating the memory ~~the~~ output signals and responsive to the memory commands, at least some of the memory modules comprising:

an insulative substrate supporting a system interface;

a plurality of memory devices disposed on the insulative substrate;

a memory hub disposed on the insulative substrate and operably coupled with the memory devices and the system interface, the memory hub managing communications between the memory devices and the system interface in response to memory commands received via the system interface;

an activity sensing device monitoring activity of the memory module containing the activity sensing device in processing memory commands, the activity sensing device being operable to generate an output corresponding thereto; and

a module power controller coupled to the activity sensing device of the memory module containing the module power controller, the module power controller being operable to direct the memory devices in the memory module containing the module power controller to a reduced power state responsive to the output of the activity sensing device indicating activity of the memory module containing the module power controller is not of a desired level.

75. (Original) The computer system of claim 74 wherein the module power controller directs the memory module to the reduced power state when the activity sensing device indicates memory module activity has fallen below the desired level.

76. (Original) The computer system of claim 74 wherein the module power controller directs the memory module to the reduced power state when the activity sensing device indicates memory module activity has exceeded the desired level.

77. (Original) The computer system of claim 74 wherein the module power controller is operable to determine when the memory module should be directed to the reduced power state responsive to the output of the activity sensing device.

78. (Original) The computer system of claim 74 wherein the module power controller is operable to direct the memory module to the reduced power state upon receiving an external reduced power signal.

79. (Original) The computer system of claim 74 wherein the module power controller of one of the memory modules comprises a master power controller, the master power controller receiving the output of the activity sensing device from at least one other memory module and, responsive to the output of the activity sensing device activity of the memory module is not of the desired level, generates an external reduced power signal to direct the at least one other memory module to the reduced power state.

80. (Original) The computer system of claim 74 wherein the memory controller comprises a master power controller, the master power controller receiving the output of the activity sensing device from at least one other memory module and, responsive to the output of the activity sensing device indicating activity of the memory module is not of the desired level, generates an external reduced power signal to direct the at least one other memory module to the reduced power state.

81. (Original) The computer system of claim 74 wherein the memory module is directed to the reduced power state by the module power controller responsive to a single indication activity of the memory module is not of the desired level reflected in the output of the activity sensing device.

82. (Original) The computer system of claim 74 wherein the memory module is directed to the reduced power state by the module power controller responsive to a plurality of indications activity of the memory module is not of the desired level reflected in the output of the activity sensing device.

83. (Original) The computer system of claim 74 wherein the memory module is directed to the reduced power state by the module power controller when the output of the activity sensing device indicates the memory module has not received a desired number of memory commands for a predetermined time period.

84. (Original) The computer system of claim 74 wherein the activity sensing device comprises an activity monitor that monitors memory commands directed to the memory module.

85. (Original) The computer system of claim 84 wherein the activity monitor monitors the memory commands received via the system interface.

86. (Original) The computer system of claim 74 wherein the activity monitor comprises part of the memory hub.

87. (Original) The computer system of claim 74 wherein the activity sensing device comprises a temperature sensor wherein the temperature sensor is operable to measure when the activity of the memory module is not of the desired level by monitoring temperature.

88. (Original) The computer system of claim 87 wherein the temperature sensor is operably coupled with at least one memory device to measure a memory device operating temperature.

89. (Original) The computer system of claim 87 wherein the temperature sensor is operably coupled with each of the memory devices to measure an aggregate memory device temperature.

90. (Original) The computer system of claim 87 wherein the temperature sensor is operably coupled with the insulative substrate to measure a memory module operating temperature.

91. (Original) The computer system of claim 87 wherein the temperature sensor is operably coupled with the memory hub to measure a memory hub operating temperature.

92. (Original) The computer system of claim 87 wherein the temperature sensor further comprises an ambient temperature sensor so that a measured temperature of the memory module can be compared to an ambient temperature.

93. (Original) The computer system of claim 74 wherein the plurality of memory devices comprise a plurality of DRAM devices.

94. (Original) The computer system of claim 93 wherein the reduced power state comprises a reduced refresh state in which memory cells of the DRAM devices are refreshed less frequently.

95. (Original) The computer system of claim 94 wherein the reduced refresh state comprises a self-refresh state.

96. (Original) The computer system of claim 74 wherein the reduced power state is a reduced response mode in which the module power controller limits response of the memory module to memory commands to control power consumption by the memory module.

97. (Original) The computer system of claim 74 wherein the module power controller limits the response of the memory module to memory commands by mandating idle intervals between responses to memory commands by the memory module.

98. (Original) The computer system of claim 74 wherein the output of the activity sensing device communicates that the memory devices of the memory module currently store no programming instructions and data, and the power management controller causes a plurality of devices of the memory module to be powered off.

99. (Original) The computer system of claim 74 wherein the output of the activity sensing device communicates that the memory devices of the memory module currently store programming information that has not been accessed by the system for an extended period, and the power management controller causes the contents of the memory devices to be saved to a storage device and a plurality of devices of the memory module to be powered off.

100. (Previously Presented) A method of controlling power used in a plurality of memory modules associated with a system, each of the memory modules containing a plurality of memory devices, the method comprising:

individually measuring activity in each of the memory modules in response to memory commands from the system in at least some of the memory modules;

determining within each of the memory modules when each of the respective memory modules is inactive based on lack of activity in response to nonrefresh memory commands from the system measured in the respective memory modules; and

internally directing the memory devices in at least one of the memory modules into a reduced power state when it is determined that activity of that memory module is not of a desired level.

101. (Original) The method of claim 100 wherein the memory module activity has fallen below the desired level.

102. (Original) The method of claim 100 wherein the memory module activity has exceeded the desired level.

103. (Original) The method of claim 100 wherein evaluating whether the memory module should be directed into the reduced power state and directing the module into the reduced power state occurs within the memory module.

104. (Original) The method of claim 100 wherein evaluating whether the memory module should be directed into the reduced power state and directing the module into the reduced power state occurs in an outside control device outside the memory module responsive to activity of the memory module not of the desired level reflected in the output of the activity sensing device.

105. (Original) The method of claim 104 wherein the outside control device resides in a memory controller.

106. (Original) The method of claim 104 wherein the outside control device resides in a system controller.

107. (Original) The method of claim 104 wherein the outside control device resides in a master memory module.

108. (Original) The method of claim 104 wherein the outside control device for other memory modules resides within the memory module.

109. (Original) The method of claim 100 wherein evaluating whether the memory module should be directed into the reduced power state is responsive to a single

occurrence of activity of the memory module not of the desired level reflected in the output of the activity sensing device.

110. (Original) The method of claim 100 wherein evaluating whether the memory module should be directed into the reduced power state is responsive to a plurality of occurrences activity of the memory module not of the desired level reflected in the output of the activity sensing device.

111. (Original) The method of claim 100 wherein evaluating whether the memory module should be directed into the reduced power state is responsive to activity of the memory module not of the desired level reflected in the output of the activity sensing measured over a predetermined time period.

112. (Original) The method of claim 111 wherein activity is measured via a memory hub of the memory module.

113. (Original) The method of claim 100 wherein evaluating whether the memory module should be directed into the reduced power state is responsive to monitoring temperature within the memory module.

114. (Original) The method of claim 113 wherein evaluating whether the memory module should be directed into the reduced power state is responsive to monitoring temperature of a memory device within the memory module.

115. (Original) The method of claim 113 wherein evaluating whether the memory module should be directed into the reduced power state is responsive to monitoring temperature of each of the memory devices within the memory module.

116. (Original) The method of claim 113 wherein evaluating whether the memory module should be directed into the reduced power state is responsive to monitoring temperature of an insulative substrate within the memory module.

117. (Original) The method of claim 113 wherein evaluating whether the memory module should be directed into the reduced power state is responsive to monitoring temperature of a memory hub.

118. (Original) The method of claim 113 further comprising measuring an ambient temperature in comparison with temperature monitored within the memory module.

119. (Original) The method of claim 100 wherein the plurality of memory devices comprise a plurality of DRAM devices and the reduced power state comprises a reduced refresh state in which memory cells of the DRAM devices are refreshed less frequently.

120. (Original) The method of claim 119 wherein the reduced refresh state is a self-refresh state.

121. (Original) The method of claim 100 wherein the reduced power state is a reduced response mode in which the module power controller limits response of the memory module to memory commands to control power consumption by the memory module.

122. (Original) The memory module of claim 121 wherein the module power controller limits the response of the memory module to memory commands by mandating idle intervals between responses to memory commands by the memory module.

123. (Original) The method of claim 100 wherein the reduced refresh state is powering off a plurality of devices of the memory module when the activity measured no programming instructions and data are stored on the memory module.

124. (Original) The method of claim 100 wherein the reduced refresh state is powering off a plurality of devices of the memory module programming information stored on the memory module has not been accessed by the system for an extended period, the contents stored in the memory module are saved to a storage device and a plurality of devices of the memory module are powered off.

125. (Previously Presented) A memory system, comprising:

a memory controller;

a memory bus operably coupled with the memory controller to communicate memory commands from the memory controller and communicate memory output signals to the memory controller; and

a plurality of memory modules operably coupled with the memory bus, the memory modules generating the memory output signals and responsive to the memory commands, at least some of the memory modules comprising:

an insulative substrate supporting a system interface;

a plurality of memory devices disposed on the insulative substrate;

a memory hub disposed on the insulative substrate and operably coupled with the memory devices and the system interface, the memory hub managing communications between the memory devices and the system interface in response to memory commands received via the system interface;

an activity sensing device monitoring activity of the memory module containing the activity sensing device in processing memory commands, the activity sensing device being operable to generate an output corresponding thereto; and

a module power controller coupled to the activity sensing device of the memory module containing the module power controller, the module power controller being operable to direct the memory module containing the module power controller to a reduced power state responsive to the output of the activity sensing device indicating activity of the memory module containing the module power controller is not of a desired level, the module power controller being operable to direct the memory module

containing the module power controller to a reduced power state by limiting the response of the memory module to memory commands.

126. (Previously Presented) The memory system of claim 125 wherein the module power controller limits the response of the memory module to memory commands by mandating idle intervals between responses to memory commands by the memory module.

127. (Currently Amended) A computer system, comprising:

a processor;

an input device, operably connected to the processor, allowing data to be entered into the computer system;

an output device, operably connected to the processor, allowing data to be output from the computer system; and

a memory system, operably coupled with the processor, the memory system comprising:

a memory controller;

a memory bus operably coupled with the memory controller to communicate memory commands from the memory controller and communicate memory output signals to the memory controller; and

a plurality of memory modules operably coupled with the memory bus, the memory modules generating the memory ~~the~~ output signals and responsive to the memory commands, at least some of the memory modules comprising:

an insulative substrate supporting a system interface;

a plurality of memory devices disposed on the insulative substrate;

a memory hub disposed on the insulative substrate and operably coupled with the memory devices and the system interface, the memory hub managing communications between the memory devices and the system interface in response to memory commands received via the system interface;

an activity sensing device monitoring activity of the memory module containing the activity sensing device in processing memory commands,

the activity sensing device being operable to generate an output corresponding thereto; and

a module power controller coupled to the activity sensing device of the memory module containing the module power controller, the module power controller being operable to direct the memory module containing the module power controller to a reduced power state responsive to the output of the activity sensing device indicating activity of the memory module containing the module power controller is not of a desired level, the module power controller being operable to direct the memory module containing the module power controller to a reduced power state by limiting the response of the memory module to memory commands.

128. (Previously Presented) The computer system of claim 127 wherein the module power controller limits the response of the memory module to memory commands by mandating idle intervals between responses to memory commands by the memory module.

129. (Currently Amended) A computer system, comprising:

a processor;

an input device, operably connected to the processor, allowing data to be entered into the computer system;

an output device, operably connected to the processor, allowing data to be output from the computer system; and

a memory system, operably coupled with the processor, the memory system comprising:

a memory controller;

a memory bus operably coupled with the memory controller to communicate memory commands from the memory controller and communicate memory output signals to the memory controller; and

a plurality of memory modules operably coupled with the memory bus, the memory modules generating the memory ~~the~~ output signals and responsive to the memory commands, at least some of the memory modules comprising:

an insulative substrate supporting a system interface;

a plurality of memory devices disposed on the insulative substrate;

a memory hub disposed on the insulative substrate and operably coupled with the memory devices and the system interface, the memory hub managing communications between the memory devices and the system interface in response to memory commands received via the system interface;

an activity sensing device monitoring monitors memory commands directed to the memory module, the activity sensing device being operable to generate an output corresponding to module activity based on the monitored memory commands; and

a module power controller coupled to the activity sensing device of the memory module containing the module power controller, the module power controller being operable to direct the memory module containing the module power controller to a reduced power state responsive to the output of the activity sensing device indicating activity of the memory module containing the module power controller is not of a desired level.

130. (Previously Presented) The computer system of claim 129 wherein the memory module is directed to the reduced power state by the module power controller when the output of the activity sensing device indicates the memory module has not received a desired number of memory commands for a predetermined time period.

131. (Previously Presented) The computer system of claim 129 wherein the activity monitor monitors the memory commands received via the system interface.